



AD-3241
Third Year B. Sc. (Sem. VI) Examination
March/April – 2015
Generic Elective for Electronics
(Integrated Circuit Technology)

Time : Hours]

[Total Marks : 50

Instructions :

(1)

<p>नीचे दृष्टावेक निशानीवाणी विगतो उत्तरवडी पर अवश्य लपवी. Fillup strictly the details of signs on your answer book.</p> <p>Name of the Examination :</p> <p>THIRD YEAR B. SC. (SEM. VI)</p> <p>Name of the Subject :</p> <p>GENERIC ELECTIVE FOR ELECTRONICS</p> <p>Subject Code No. : 3 2 4 1 Section No. (1, 2,.....): Nil</p>	<p>Seat No. :</p> <table border="1" style="width: 100%; height: 20px;"><tr><td style="width: 15%;"></td><td style="width: 15%;"></td><td style="width: 15%;"></td><td style="width: 15%;"></td><td style="width: 15%;"></td><td style="width: 15%;"></td></tr></table> <div style="border: 1px solid black; border-radius: 15px; padding: 10px; text-align: center; margin-top: 10px;">Student's Signature</div>						

- (2) Figures to the right indicate full marks.
- (3) Assume data wherever necessary.
- (4) Use suitable examples.

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|---|---|---|
| 1 | Write very short answers : | 8 |
| | (1) Give full form of VLSI and IC. | |
| | (2) What is EGS and MGS with respect to IC technology ? | |
| | (3) What is the meaning of epitaxial growth ? | |
| | (4) Give the physical dimensions of SSI, MSI, LSI, VLSI. | |
| 2 | (A) What is the meaning of seed crystal? How is it used to pull the ingot using the CZ method | 7 |
| | (B) Discuss the CVD (Chemical Vapour Deposition) Method | 7 |

OR

2	(A) Design using planer technology a circuit of your choice.	7
	(B) Describe the method to dope silicon wafer by ion-implantation.	7
3	(A) How are monolithic diodes and bipolar junction transistors integrated.	8
	(B) How are monolithic resistors integrated what are the limitations of integrating a resistor on a chip.	6
OR		
3	(A) Give the steps to process planer IC. Give the layers and the thickness of planer technology.	9
	(B) Write a brief description of diffusion growth process	5
4	Write Short Notes :	14
	(1) Photolithography	
	(2) X-ray and ion beam lithography	
	(3) Oxidation of wafer	
	(4) Epitaxial growth	
