Instructions:

(1) Fill up strictly the details of signs on your answer book.

2. All 28 questions are compulsory.
3. All symbols and abbreviations have their usual meaning.
4. Figures to right indicate full marks.
5. Non-programmable calculators are allowed.
6. Assume data if necessary.

Q. 1 to 12 Multiple choice questions : (1 mark)
Q. 13 to 22 Multiple Choose Questions : (2 marks)
Q. 23 to 28 Multiple Choice Questions : (3 marks)

O.M.R. Sheet क्षण अंगेल, असंश्लील सुविधाओ आपेक्ष...
O.M.R. Sheet-ली पाणि अपेक्ष छ.
Important instructions to fill up O.M.R. Sheet are given back side of provided O.M.R. Sheet.
1 Which of the following condition not allowed in S-R flip-flop using NOR gates?
(A) S=1, R=0
(B) S=1, R=1
(C) S=0, R=0
(D) S=0, R=1

2 Which type of ROM can be erased by an electrical signal?
(A) EPROM
(B) EEPROM
(C) ROM
(D) mask ROM

3 Which type of ROM has to be custom built by the factory?
(A) EPROM
(B) None of these
(C) ROM
(D) mask ROM

4 ABCD counter is a ________
(A) decade counter
(B) MOD-16 counter
(C) binary counter
(D) full-modulus counter

5 To serially shift a nibble (four bits) of data into a shift register, there must be ______.
(A) eight clock pulses
(B) one clock pulse for each 1 in the data
(C) one clock pulse
(D) four clock pulses

6 What is one disadvantage of an S-R flip flop?
(A) It has no clock input
(B) It has only a single output
(C) It has no enable input
(D) It has an invalid state
7 How many flip-flops are required to make a MOD-32 binary counter?
   (A) 5
   (B) 6
   (C) 3
   (D) 45

8 In sequential circuits the present input depends on
   (A) present as well as past inputs
   (B) None of these
   (C) past input only
   (D) present input only

9 When two counters are cascaded, the overall MOD number is equal to the _____ of their individual MOD numbers.
   (A) log
   (B) reciprocal
   (C) product
   (D) sum

10 The main difference between JK and RS flip-flop is that
    (A) JK flip-flop accepts both inputs as 1
    (B) JK flip-flop is acronym of junction cathode multivibrator
    (C) JK flip-flop does not need a clock pulse
    (D) There is feedback in JK flip-flop

11 A flip-flop has two outputs which are
    (A) always complementary
    (B) all of these stated
    (C) always 0
    (D) always 1

12 Master-slave configuration is used in flip flops to
    (A) eliminate the race round condition
    (B) improve the reliability
    (C) increase its clock rate
    (D) reduce power dissipation
13 What is meant by parallel-loading the register?

(A) Momentarily disabling the synchronous SET and RESET inputs

(B) Shifting the data in all flip-flops simultaneously

(C) Loading data in all four flip-flops at the same time

(D) Loading data in two of the flip-flops

14 What happens to the output in an asynchronous binary down counter whenever a clock pulse occurs?

(A) The output word decreases by 1

(B) The output word decreases by 2

(C) The output word increases by 1

(D) The output word increases by 2

15 Which of the following best describes the action of pulse-triggered FF’s?

(A) A pulse on the clock transfers data from input to output

(B) The synchronous inputs must be pulsed

(C) The clock and the S-R inputs must be pulse shaped

(D) The data is entered on the leading edge of the clock, and transferred out on the trailing edge of the clock.

DF-2991_C] 4 [ Contd...
16 An invalid condition in the operation of an active-HIGH input S-R latch occurs when _______.

(A) a LOW is applied to the S input while a HIGH is applied to the R input
(B) a HIGH is applied to the S input while a LOW is applied to the R input
(C) HIGHs are applied simultaneously to both inputs S and R
(D) LOWs are applied simultaneously to both inputs S and R

17 As a general rule for stable flip-flop triggering the clock pulse rise and fall times must be “.

(A) at a maximum value to enable the input control signals to stabilize
(B) of no consequence as long as the levels are within the determinate range of value
(C) very long
(D) very short

18 The group of bits 11001 is serially shifted (right-most bit first) into a 5-bit parallel output shift register with an initial state 01110. After three clock pulses, the register contains _______.

(A) 00101
(B) 00110
(C) 01110
(D) 00001
19 A 4-bit parallel access shift register can be used for _______.
   (A) parallel in/serial out operation
   (B) All of these
   (C) serial in/serial out operation
   (D) serial in/parallel out operation

20 Synchronous counters eliminate the delay problems encountered with asynchronous counters because the:
   (A) input clock pulses are not used to activate any of the counter stages
   (B) input clock pulses are applied simultaneously to each stage
   (C) input clock pulses are applied only to the first and last stages
   (D) input clock pulses are applied only to the last stage

21 What is the difference between a 7490 and a 7492?
   (A) 7490 is a MOD-16, 7492 is a MOD-10
   (B) 7490 is a MOD-10, 7492 is a MOD-12
   (C) 7490 is a MOD-12, 7492 is a MOD-10
   (D) 7490 is a MOD-12, 7492 is a MOD-16

22 What type of register would shift a complete binary number in one bit at a time and shift all the stored bits out one bit at a time?
   (A) SIPO
   (B) PIPO
   (C) PISO
   (D) SISO
A 4 bit binary ripple counter and 4 bit synchronous counter uses with propagation delay time of 50 ns each. The possible maximum delay time required for the change the state will be for 4 bit ripple counter is _____ ns and for 4 bit synchronous counter is _____ ns.

(A) 100, 100
(B) 200, 200
(C) 50, 50
(D) 200, 50

The bit sequence 10011100 is serially entered (right-most bit first) into an 8-bit parallel out shift register that is initially clear. What are the Q outputs after four clock pulses ?

(A) 00001100
(B) 11110000
(C) 10011100
(D) 11000000

Four J-K flip-flops are cascaded with their J-K inputs tied HIGH. If the input frequency (fin) to the first flip-flop is 32 kHz, the output frequency (fout) is _______.

(A) 4 kHz
(B) 16 kHz
(C) 1 kHz
(D) 2 kHz
26 A bidirectional 4-bit shift register is storing the nibble 1101. Its input is HIGH. The nibble 1011 is waiting to be entered on the serial data-input line. After three clock pulses, the shift register is storing ________.

(A) 0001
(B) 1110
(C) 1101
(D) 0111

27 A MOD-16 ripple counter is holding the count $1001_2$. What will the count be after 31 clock pulses?

(A) $1011_2$
(B) $1101_2$
(C) $1000_2$
(D) $1010_2$

28 What decimal value is required to produce an output at “X”?

(A) 2
(B) 5
(C) 1
(D) 1 or 4