



DF-2991

Second Year B. Sc. (Sem. III) Examination

March / April - 2016

Electronics : Paper - IV

(Advance Digital Electronics & Circuit Design)

Time : 2 Hours]

[Total Marks : 50

Instructions :

(1)

નીચે દર્શાવેલ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી. Fillup strictly the details of signs on your answer book.	Seat No. :
Name of the Examination :	<input type="text"/>
SECOND YEAR B. Sc. (SEM. 3)	<input type="text"/>
Name of the Subject :	<input type="text"/>
ELECTRONICS - 4	<input type="text"/>
Subject Code No. : <input type="text" value="2"/> <input type="text" value="9"/> <input type="text" value="9"/> <input type="text" value="1"/>	<input type="text"/>
Section No. (1, 2,.....) : <input type="text" value="1"/>	
	Student's Signature

- (2) All 28 questions are compulsory.
- (3) All symbols and abbreviations have their usual meaning.
- (4) Figures to right indicate full marks.
- (5) Non-programmable calculators are allowed.
- (6) Assume data if necessary.

Q. 1 to 12 Multiple choice questions : (1 mark)

Q. 13 to 22 Multiple Choice Questions : (2 marks)

Q. 23 to 28 Multiple Choice Questions : (3 marks)

***O.M.R. Sheet ભરવા અંગેની અગત્યની સૂચનાઓ આપેલ
O.M.R. Sheet-ની પાછળ છાપેલ છે.***

***Important instructions to fillup O.M.R. Sheet
are given back side of provided O.M.R. Sheet.***

- 1 In sequential circuits the present input depends on
 - (A) present input only
 - (B) present as well as past inputs
 - (C) None of these
 - (D) past input only

- 2 When two counters are cascaded, the overall MOD number is equal to the _____ of their individual MOD numbers.
 - (A) sum
 - (B) log
 - (C) reciprocal
 - (D) product

- 3 The main difference between JK and RS flip-flop is that
 - (A) There is feedback in JK flip-flop
 - (B) JK flip-flop accepts both inputs as 1
 - (C) JK flip-flop is acronym of junction cathode multivibrator
 - (D) JK flip-flop does not need a clock pulse

- 4 A flip-flop has two outputs which are
 - (A) always 1
 - (B) always complementary
 - (C) all of these stated
 - (D) always 0

- 5 Master-slave configuration is used in flip flops to
 - (A) reduce power dissipation
 - (B) eliminate the race round condition
 - (C) improve the reliability
 - (D) increase its clock rate

- 6 Which of the following condition not allowed in S-R flip-flop using NOR gates ?
 - (A) $S=0, R=1$
 - (B) $S=1, R=0$
 - (C) $S=1, R=1$
 - (D) $S=0, R=0$

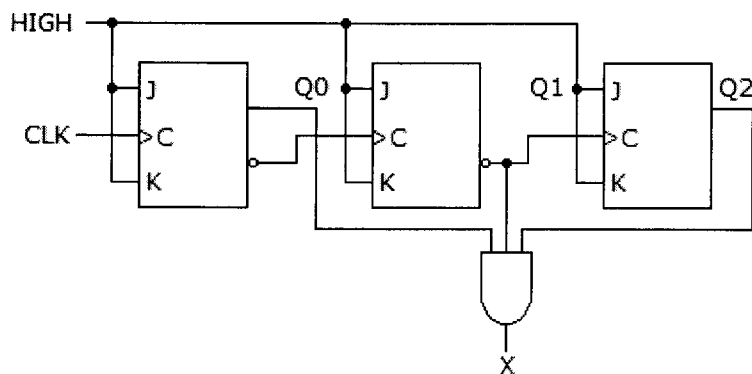
- 7 Which type of ROM can be erased by an electrical signal ?
(A) mask ROM
(B) EPROM
(C) EEPROM
(D) ROM
- 8 Which type of ROM has to be custom built by the factory ?
(A) mask ROM
(B) EPROM
(C) None of these
(D) ROM
- 9 ABCD counter is a _____
(A) full-modulus counter
(B) decade counter
(C) MOD-16 counter
(D) binary counter
- 10 To serially shift a nibble (four bits) of data into a shift register, there must be _____.
(A) four clock pulses
(B) eight clock pulses
(C) one clock pulse for each 1 in the data
(D) one clock pulse
- 11 What is one disadvantage of an S-R flip flop ?
(A) It has an invalid state
(B) It has no clock input
(C) It has only a single output
(D) It has no enable input
- 12 How many flip-flops are required to make a MOD-32 binary counter ?
(A) 45
(B) 5
(C) 6
(D) 3

- 13 As a general rule for stable flip-flop triggering the clock pulse rise and fall times must be “:
- (A) very short
 - (B) at a maximum value to enable the input control signals to stabilize
 - (C) of no consequence as long as the levels are within the determinate range of value
 - (D) very long
- 14 The group of bits 11001 is serially shifted (right-most bit first) into a 5-bit parallel output shift register with an initial state 01110. After three clock pulses, the register contains _____.
- (A) 00001
 - (B) 00101
 - (C) 00110
 - (D) 01110
- 15 A 4-bit parallel access shift register can be used for _____.
- (A) serial in/parallel out operation
 - (B) parallel in/serial out operation
 - (C) All of these
 - (D) serial in/serial out operation

- 16 Synchronous counters eliminate the delay problems encountered with asynchronous counters because the :
- (A) input clock pulses are applied only to the last stage
 - (B) input clock pulses are not used to activate any of the counter stages
 - (C) input clock pulses are applied simultaneously to each stage
 - (D) input clock pulses are applied only to the first and last stages
- 17 What is the difference between a 7490 and a 7492 ?
- (A) 7490 is a MOD-12, 7492 is a MOD-16
 - (B) 7490 is a MOD-16, 7492 is a MOD-10
 - (C) 7490 is a MOD-10, 7492 is a MOD-12
 - (D) 7490 is a MOD-12, 7492 is a MOD-10
- 18 What type of register would shift a complete binary number in one bit at a time and shift all the stored bits out one bit at a time?
- (A) SISO
 - (B) SIPO
 - (C) PIPO
 - (D) PISO
- 19 What is meant by parallel-loading the register ?
- (A) Loading data in two of the flip-flops
 - (B) Momentarily disabling the synchronous SET and RESET inputs
 - (C) Shifting the data in all flip-flops simultaneously
 - (D) Loading data in all four flip-flops at the same time

- 20 What happens to the output in an asynchronous binary down counter whenever a clock pulse occurs ?
- (A) The output word increases by 2
 - (B) The output word decreases by 1
 - (C) The output word decreases by 2
 - (D) The output word increases by 1
- 21 Which of the following best describes the action of pulse-triggered FF's ?
- (A) The data is entered on the leading edge of the clock, and transferred out on the trailing edge of the clock.
 - (B) A pulse on the clock transfers data from input to output
 - (C) The synchronous inputs must be pulsed
 - (D) The clock and the S-R inputs must be pulse shaped
- 22 An invalid condition in the operation of an active-HIGH input S-R latch occurs when _____.
- (A) LOWs are applied simultaneously to both inputs S and R
 - (B) a LOW is applied to the S input while a HIGH is applied to the R input
 - (C) a HIGH is applied to the S input while a LOW is applied to the R input
 - (D) HIGHs are applied simultaneously to both inputs S and R

- 23 A bidirectional 4-bit shift register is storing the nibble 1101. Its input is HIGH. The nibble 1011 is waiting to be entered on the serial data-input line. After three clock pulses, the shift register is storing _____.
- (A) 0111
 (B) 0001
 (C) 1110
 (D) 1101
- 24 A MOD-16 ripple counter is holding the count 1001_2 . What will the count be after 31 clock pulses ?
- (A) 1010_2
 (B) 1011_2
 (C) 1101_2
 (D) 1000_2
- 25 What decimal value is required to produce an output at "X" ?



- (A) 1 or 4
 (B) 2
 (C) 5
 (D) 1

- 26 A 4 bit binary ripple counter and 4 bit synchronous counter uses with propagation delay time of 50 ns each. The possible maximum delay time required for the change the state will be for 4 bit ripple counter is _____ ns and for 4 bit synchronous counter is _____ ns.
- (A) 200, 50
- (B) 100, 100
- (C) 200, 200
- (D) 50, 50
- 27 The bit sequence 10011100 is serially entered (right-most bit first) into an 8-bit parallel out shift register that is initially clear. What are the Q outputs after four clock pulses ?
- (A) 11000000
- (B) 00001100
- (C) 11110000
- (D) 10011100
- 28 Four J-K flip-flops are cascaded with their J-K inputs tied HIGH. If the input frequency (f_{in}) to the first flip-flop is 32 kHz, the output frequency (f_{out}) is _____.
- (A) 2 kHz
- (B) 4 kHz
- (C) 16 kHz
- (D) 1 kHz

