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DF-2991

Second Year B. Sc. (Sem. III) Examination

March / April - 2016

Electronics : Paper - IV

(Advance Digital Electronics & Circuit Design)

Time : **2** Hours] [Total Marks : **50**

Instructions :

(1)

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fillup strictly the details of ☛ signs on your answer book.

Name of the Examination :

☛ SECOND YEAR B. Sc. (SEM. 3)

Name of the Subject :

☛ ELECTRONICS - 4

☛ Subject Code No. : 2 9 9 1 ☛ Section No. (1, 2,.....) : 1

Seat No. :

Student's Signature

(2) All 28 questions are compulsory.

(3) All symbols and abbreviations have their ususal meaning.

(4) Figures to right indicate full marks.

(5) Non-programmable calculators are allowed.

(6) Assume data if necessary.

Q. 1 to 12 Multiple choice questions : (1 mark)

Q. 13 to 22 Multiple Choise Questions : (2 marks)

Q. 23 to 28 Multiple Choice Questions : (3 marks)

***O.M.R. Sheet* ભરવા અંગેની અગત્યની સૂચનાઓ આપેલ *O.M.R. Sheet*ની પાછળ છાપેલ છે.**

Important instructions to fillup O.M.R. Sheet are given back side of provided O.M.R. Sheet.

1 The main difference between JK and RS fip-flop is that
(A) JK flip-flop does not need a clock pulse
(B) There is feedback in JK flip-flop
(C) JK flip-flop accepts both inputs as 1
(D) JK flip-flop is acronym of junction cathode multivibrator

2 A flip-flop has two out puts which are
(A) always 0
(B) always 1
(C) always complementary
(D) all of these stated

3 Master-slave configuration is used in flip flops to
(A) increase its clock rate
(B) reduce power dissipation
(C) eliminate the race round condition
(D) improve the reliability

4 Which of the following condition not allowed in S-R flip-flop using NOR gates ?
(A) S=0, R=0
(B) S=0, R=1
(C) S=1, R=0
(D) S=1, R=1

5 Which type of ROM can be erased by an electrical signal ?
(A) ROM
(B) mask ROM
(C) EPROM
(D) EEPROM

6 Which type of ROM has to be custom built by the factory ?
(A) ROM
(B) mask ROM
(C) EPROM
(D) None of these

7 ABCD counter is a _____

(A) binary counter

(B) full-modulus counter

(C) decade counter

(D) MOD-16 counter

8 To serially shift a nibble (four bits) of data into a shift register, there must be _____.

(A) one clock pulse

(B) four clock pulses

(C) eight clock pulses

(D) one clock pulse for each 1 in the data

9 What is one disadvantage of an S-R flip flop ?

(A) It has no enable input

(B) It has an invalid state

(C) It has no clock input

(D) It has only a single output

10 How many flip-flops are required to make a MOD-32 binary counter ?

(A) 3

(B) 45

(C) 5

(D) 6

11 In sequential circuits the present input depends on

(A) past input only

(B) present input only

(C) present as well as past inputs

(D) None of these

12 When two counters are cascaded, the overall MOD number is equal to the _____ of their individual MOD numbers.

(A) product

(B) sum

(C) log

(D) reciprocal

13 Which of the following best describes the action of pulse-triggered FF's ?

(A) The clock and the S-R inputs must be pulse shaped

(B) The data is entered on the leading edge of the clock, and transferred out on the trailing edsge of the clock.

(C) A pulse on the clock transfers data from input to output

(D) The synchronous inputs must be pulsed

14 An invalid condition in the operation of an active-HIGH input S-R latch occurs when _____.

(A) HIGHs are applied simultaneously to both inputs S and R

(B) LOWs are applied simultaneously to both inputs S and R

(C) a LOW is applied to the S input while a HIGH is applied to the R input

(D) a HIGH is applied to the S input while a LOW is applied to the R input

15 As a general rule for stable flip-flop triggering the clock pulse rise and fall times must be ":

(A) very long

(B) very short

(C) at a maximum value to enable the input control signals to stabilize

(D) of no consequence as long as the levels are within the determinate range of value

16 The group of bits 11001 is serially shifted (right-most bit first) into a 5-bit parallel output shift register with an initial state 01110. After three clock pulses, the register contains _____.

(A) 01110

(B) 00001

(C) 00101

(D) 00110

17 A 4-bit parallel access shift register can be used for _____.

(A) serial in/serial out operation

(B) serial in/parallel out operation

(C) parallel in/serial out operation

(D) All of these

18 Synchronous counters eliminate the delay problems encountered with asynchronous counters because the :

(A) input clock pulses are applied only to the first and last stages

(B) input clock pulses are applied only to the last stage

(C) input clock pulses are not used to activate any of the counter stages

(D) input clock pulses are applied simultaneously to each stage

19 What is the difference between a 7490 and a 7492 ?

(A) 7490 is a MOD-12, 7492 is a MOD-10

(B) 7490 is a MOD-12, 7492 is a MOD-16

(C) 7490 is a MOD-16, 7492 is a MOD-10

(D) 7490 is a MOD-10, 7492 is a MOD-12

20 What type of register would shift a complete binary number in one bit at a time and shift all the stored bits out one bit at a time?

(A) PISO

(B) SISO

(C) SIPO

(D) PIPO

21 What is meant by parallel-loading the register ?

(A) Loading data in all four flip-flops at the same time

(B) Loading data in two of the flip-flops

(C) Momentarily disabling the synchronous SET and RESET inputs

(D) Shifting the data in all flip-flops simultaneously

22 What happens to the output in an asynchronous binary down counter whenever a clock pulse occurs ?

(A) The output word increases by 1

(B) The output word increases by 2

(C) The output word decreases by 1

(D) The output word decreases by 2

23 Four J-K flip-flops are cascaded with their J-K inputs tied HIGH. If the input frequency (fin) to the first flip-flop is 32 kHz, the output frequency (fout) is _____.

(A) 1 kHz

(B) 2 kHz

(C) 4 kHz

(D) 16 kHz

24 A bidirectional 4-bit shift register is storing the nibble 1101. Its input is HIGH. The nibble 1011 is waiting to be entered on the serial data-input line. After three clock pulses, the shift register is storing _____.

(A) 1101

(B) 0111

(C) 0001

(D) 1110

25 A MOD-16 ripple counter is holding the count 1001_2. What will the count be after 31 clock pulses ?

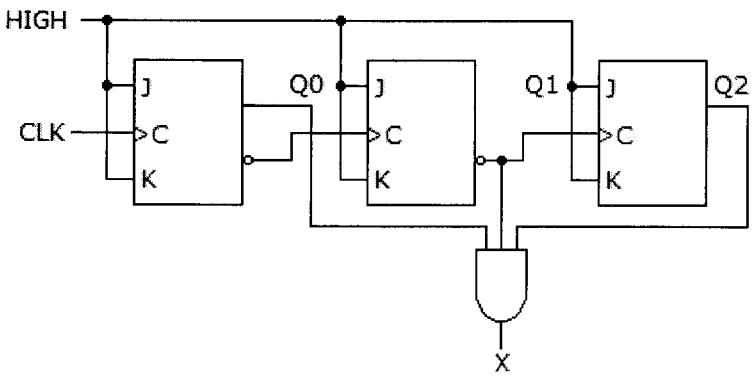
(A) 1000_2

(B) 1010_2

(C) 1011_2

(D) 1101_2

26 What decimal value is required to produce an output at "X" ?



(A) 1

(B) 1 or 4

(C) 2

(D) 5

27 A 4 bit binary ripple counter and 4 bit synchronous counter uses with propagation delay time of 50 ns each. The possible maximum delay time required for the change the state will be for 4 bit ripple counter is _____ ns and for 4 bit synchronous counter is _____ns.

(A) 50, 50

(B) 200, 50

(C) 100, 100

(D) 200, 200

28 The bit sequence 10011100 is serially entered (right-most bit first) into an 8-bit parallel out shift register that is initially clear. What are the Q outputs after four clock pulses ?

(A) 10011100

(B) 11000000

(C) 00001100

(D) 11110000